Course Number and Title:	EEE 3310 Digital Electronics			
Credit Hours:	3 credits: Lectures 3 Hours, Lab: 0			
Current Academic Term:	Fall 2018			
Office:	Room # IST-2097			
Office Hours:	Hours: Tuesday and Thursday: 10:00-11:00 am, 3:00-5:00pm; Wednesday: 2:00-3:00 pm, or just stop by if not busy, or unavailable, contact the instructor for a mutually convenient time.			
Office Phone:	Tel: (863)-874-8647			
Email:	asargolzaei@floridapoly.edu			
Class Meeting Day, Time & Location:	Tuesday and Thursday: 8:00– 9:15 am. Room # IST-1015			
Course Website:	Canvas			
Official Catalog Course Description:	This course focuses on the implementation of logic devices, MOSFET's, and BJT's. Students will analyze logic families including NMOS, CMOS, and TTL. The fundamentals of digital memory circuits will be covered.			
Prerequisite(s):	EEL 3111C - Circuits 1 EEL 3702C - Digital Logic Design			
Pre-Requisite Policy	• The pre-requisite(s) and co-requisite(s) of a course as indicated in the course catalog will be strictly enforced, without exception. • A student who completes a course without first completing its prerequisites will be required to retake the class regardless of the grade received for the course.			
Gordon Rule:	NO			
Required Texts:	1- M. H. Rashid. (2017). Microelectronic Circuits - Analysis and Design, 3rd edition, Cengage Publishing. 2- Microelectronic Circuits, Sedra & Smith, Oxford University Press, 6th edition, 2010, (ISBN-10: 0195323033, ISBN-13: 9780195323030).			
Instructional Materials"	PowerPoint slides and in class lectures			
Equipment and Materials:	Students need to be familiar with PSPISE or MATLAB Simulink or MultiSim			
Course Objectives:	At the end of this course, you should be able to: • Introduce the operation of transistors as switches to implement the binary states of a logic circuit are normally represented by two distinct voltages. • Covers the realization of switching function by a MOS transistors. • Covers the parameters and performance criteria for analysis and design of logic gates. • Covers the comparative performance and evaluations of MOS logic gates. • Covers the fundamentals of digital memory circuits.			
Course Learning Outcomes (CLOs):	**#**	After successfully completing the course with a grade of C (2.0/4.0) or better, the student should be able to do the following:	**Learning level**	**ABET Criteria**
	1.	Apply modern simulation tool such as SPISE and MATLAB for evaluation of NMOS, CMOS and MOSFETs characteristics and performances along with laboratorial activity	3	k

	2.	Design CMOS logic inverter, NMOS logic inverter with load	5	e
	3.	Design and analyze of MOS inverters and logic gates	5	e, c
	4.	Design logic gates and memory cells at the transistor level	5	c
	5.	Identify a contemporary issue on digital electronics and applications.	6	h, i, j

Attendance	Attendance - see also University Policy at https://floridapolytechnic.org/wp-content/uploads/FPU-5.0010AP-Student-Attendance.pdf *Course specific attendance requirement:* Students are expected to attend class. Students whose absences exceed 8 classes may be Administratively Withdrawn at the discretion of the instructor unless prior arrangement is made to accommodate special circumstances.
Grading Scale:	See also University Policy https://floridapolytechnic.org/wp-content/uploads/FPU-5.0071AP-Grading-Policy-10.20.15.pdf

0	55	58	63	67	70	73	77	80	83	87	90
F	D-	D	D+	C-	C	C+	B-	B	B+	A-	A

Assignment/Evaluation Methods:	Grade items: Quizzes, assignments, and Final Exam throughout the semester after the completion of a specific topic area – see the schedule for more details.	Points
	Project	20
	Homework	20
	Exam 1	20
	Exam 2	20
	Exam 3	20
	Total	100

Make-Up:	No makeup tests or quizzes, except in case of emergency, e.g. illness and accident. For makeup tests, medical certificate is required, and the instructor must be notified in advance of the test.
Final Grade Calculations	The CANVAS calculates and displays the final letter grade based on the weighting factors as listed under **Assignment/Evaluation Methods**
Academic Support Resources	**Library**: Students can access the Florida Polytechnic University Library through the student portal Pulse and Canvas, on and off campus. Students may direct questions to the Success Desk in the Commons or by email, library@floridapoly.edu. **ASC**: The Academic Success Center, located in the Commons and at ASC East, provides a range of services. Students may direct questions to success@floridapoly.edu.

University Policies	**Academic Integrity**: All students must commit to the highest ethical standards in completion of all academic pursuits and endeavors: Academic Integrity **Reasonable Accommodations**: Students who qualify for course or classroom adjustments under the Americans with Disabilities Act (ADA) must register with the Office of Disability Services: Request for Disability Services. **Accommodations for** Religious Observances, Practices and Beliefs **Title IX**: Florida Polytechnic University is committed to ensuring a safe, productive learning environment on our campus that prohibits sexual misconduct, including discrimination based on sex or gender, harassment, stalking, sexual assault, sexual exploitation, or intimate partner violence. If you or someone you know needs assistance, you may speak to any university employee; however, they have an obligation to report the incident to the Title IX Coordinator, who will keep that information private to the greatest extent possible. If you want to speak to someone permitted to keep your disclosure confidential, seek assistance from the Florida Polytechnic University Ombudsman, BayCare's Student Assistance Program, 1-800-878-5470 and locally within the community at Peace River Center, 863-412-2700 (24-hour hotline) or 863-412-2708 to schedule an appointment. If you or someone you know feels unsafe or may be in imminent danger, please call the Florida Polytechnic University Police Department 863-874-8472 or the local Police Department 911 immediately. For more information about policy, reporting options and resources at Florida Polytechnic University and the community, please visit the Title IX Website.
Topics to be covered	This course thoroughly investigates the fundamentals in design and analysis of MOS integrated circuits. The topics to be covered include: 1. Binary numbers and Boolean Algebra 2. MOS transistor 3. Static characteristics of MOS circuits 4. Dynamic characteristics of MOS circuits 5. Combinational MOS logic circuits 6. Sequential MOS logic circuits 7. Dynamic logic circuits 8. Semiconductor memories 9. Low-power CMOS logic circuit design
Expectations From Students	• Read the complete syllabus and the deadlines. • Submit assignments in the CANVAS by the due dates (normally one week after posting date) to avoid any grade penalty.
Tentative Dates and Schedule	• Final Exam is scheduled on the final exam week and is announced by the university. • Other importance dates will be posted in the CANVAS. Students need to check the CANVAS at least twice a week.
Exam policy	• Make sure to complete the assigned homework in order to do well in the exam. • No discussion is permitted during the exams. • Instructor is not compelled to give credit for something he cannot read or follow logically. • Cheating is considered as a serious offense. Students who are caught will receive the appropriate consequences.

Class policy	• **Attendance:** Attendance in the course is **mandatory** and student is not allowed to miss any class during the semester. • **Academic Misconduct:** For work submitted, it is expected that each student will submit their own original work. Any evidence of duplication, cheating or plagiarism will result at least a failing grade for the course. • **Excused Absences:** Only emergency medical situations or extenuating circumstances are excused with proper documentation. After reviewing documentation, you are required to email a description of the excuse and absence dates as a written record to asargolzaei@floridapoly.edu. • Students are encouraged to ask questions and to discuss course topics with the instructor and with each other. • **Any work submitted should display ID number and should be signed, as the students' own work, and that no unauthorized help was obtained.** • Cell phones, communicators, MP3 players, head sets are not allowed to be used in the class. • **DO NOT** send assignments by email. • Instructor reserves right to change course materials, date, and schedules as necessary. These changed will be announced in the classroom and/or CANVAS.
Expectations from The Faculty	• Assignment or Homework is always graded within 1 week of being turned in and solution will be posted by that time. • Exams are always graded and returned with 1 week of the examination date. • Response to any questions by e-mail or phone within 48 hours (expect Weekends, breaks, and holidays).
Special Notes and instructions:	• All assignments must be turned-in on time. Late home works will **NOT** be accepted. • All reports must the submitted in PDF files at the CANVAS site unless otherwise stated. No-high resolution images of assignments. • DO NOT send assignments by e-mails. The CANVAS drop box is the only place to submit your assignments • Students are expected to spend at least two hours completing "out of class student work" for each hour in class. All out of class work will be graded and will comprise the percentage of the final course grade. • Last not the least, when you e-mail to the instructor, you must mention the course number in your note.

Created by:	Dr. Arman Sargolzaei	08/17//2016
Last Modified:	Dr. Arman Sargolzaei	08/17//2018
Reviewed by:	Dr. Muhammad H Rashid	08/20/2018

TENTATIVE SCHEDULE

weeks	Date	**Reading - Sections**	**Topics**	**Classes**	**Assignments**
1.	Aug 22-26		Read course syllabus and familiarize with CANVAS.	1	Quiz
2.	Aug 27 –Sep 2	M1	Review of logic design Introduction to digital electronics	2	
3.	Sep 3 – 9	M2	MOSFET transistor	2	1
4.	Sep 10 – 16	M2	Logic gate design using MOSFET	2	2
5.	Sep 17 – 23	M3	Logic design circuit using Bipolar Junction Transistor (BJT)	2	3
6.	Sep 24 – 30	M4	Logic inverter design Voltage transfer characteristics of a MOS	2	Exam 1
7.	Oct 1 - 7	M4	CMOS digital logic circuits	2	4
8.	Oct 8 – 14	M4	Voltage transfer characteristics of CMOS	2	
9.	Oct 15 – 21	M5	Advanced MOS and Bipolar Logic Circuits	2	5
10.	Oct 22 – 28	M6	Problem solving and transistor sizing	2	Midterm survey
11.	Oct 29 – Nov 4	M7	CMOS Implementation of SR Flip-Flops D Flip-Flop Circuits	2	Exam 2
12.	Nov 5 – 11	M7	Semiconductor Memories Static Memory Cell Structure	2	6
13.	Nov 12 – 18	M7	Dynamic Memory Cell Sense Amplifiers and Address Decoders Operation of A Sense Amplifier	2	
14.	Nov 19 – 25	M7	The Row-Address Decoder The Column-Address Decoder	1	7
15.	Nov 26– Dec 2	M7	MOS ROM design	2	
16.	Dec 3 – 5	M8	Problem solving	1	Project
17.	Dec 6 – 7	Reading Days		0	
	Dec 8 – 13		Exam 3	1	
			Total	30	

WITHTHDRWAL DATE WITHOUT ACADEMIC PENALTY DEADLINE (W ASSIGNED): NOVEMBER 19, 2018